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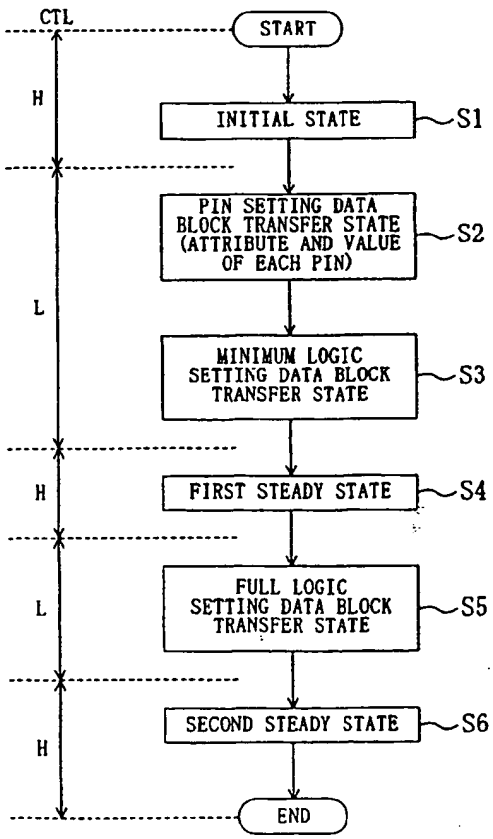
(54) PROGRAMMABLE LOGIC DEVICE AND PROGRAMMING METHOD

(57) Pin setting data for defining initial states of external pins of a programmable logic device (PLD) is transferred to the PLD to set all the external pins before logic setting data for the PLD is transferred from memory, thereby preventing an unstable state of the PLD from propagating to logic circuits adjacent to the PLD. The logic setting data is divided into minimum logic setting data for defining functions required for a stable operation of a system and full logic setting data for defining all functions of the PLD, including functions other than the functions required for a stable operation of the system, and the former is transferred before the latter to reduce a period in which the PLD is unstable during the startup of the system, thereby avoiding instability during the system startup when the PLD is incorporated into an existing system.

Fig. 5



EP 1 235 351 A1

Description

TECHNICAL FIELD

[0001] The present invention relates to a programmable logic device (PLD) and a programming method thereof.

BACKGROUND ART

[0002] Today, PLDs of which the circuit configuration can be programmed at will are widely used. Program data is stored in a memory area within the PLD or external memory. The program data is transferred to an internal logic circuit to provide function settings of the PLD when the PLD is powered up or reset.

[0003] An example of the PLD is described in US patent No. 4,870,302 in which configuration of its internal logic circuits (including wiring) can be programmed at will.

[0004] The first state of a prior-art PLD is the initial state during power-up, the second state is a program data transfer state, and the third state is a steady state. The states of the external pins and internal circuit of the PLD are unstable until the second state (transfer state) is finished. The states of the external pins and internal logic circuit do not become stable until the PLD enters a steady state after all program data is transferred to it.

[0005] The larger the size of the PLD circuit, the longer the period of the second state (transfer state) and therefore the longer a period during which the states of the external pins and internal logic circuit are unstable. In the prior art, the unstable state propagates to logic circuits adjacent to the PLD, decreasing the stability of the entire system. Especially in a configuration in which the PLD is connected to a bus within an electronic circuit system such as a personal computer, the entire system can be initialized only after the state of the PLD becomes stable during the startup of the system. Therefore it is difficult to connect the PLD to the bus in the system that has an existing, predefined startup sequence.

[0006] To avoid the above-described unstable state, a transceiver may be provided between the PLD and a logic circuit to prohibit the propagation of the unstable state. However, this approach has problems that connection delay time increases as the number of components increases, and the logic circuit cannot reference the state of the PLD until the state of the PLD becomes stable.

DISCLOSURE OF THE INVENTION

[0007] The present invention has been made in the light of the above-described problems and it is an object of the present invention to reduce the period of time in which the state of a PLD is unstable after system startup.

[0008] To solve the problems, according to the present invention, program data is divided into a pin setting data block for defining an initial state of ach of a plurality of external pins and a logic setting data block for defining functions of internal logic circuits, and a PLD receives the pin setting data block before the logic setting data block. This allows the states of the external pins to become stable earlier during system startup.

[0009] According to the present invention, the PLD receives a minimum logic setting data block for defining functions (functions required for a stable operation of the system) of some of its internal logic circuits required for system startup before receiving a full logic setting data block for defining functions of all of its internal logic circuits. This allows logic circuits adjacent to the PLD to reference the state of the PLD earlier during system startup.

BRIEF DESCRIPTION OF DRAWINGS

[0010]

Fig. 1 is a block diagram showing an exemplary configuration of a system using a PLD according to the present invention;
Fig. 2 is a block diagram showing an exemplary internal configuration of the PLD shown in Fig. 1;
Fig. 3 is a block diagram showing an exemplary internal configuration of a logic array shown in Fig. 2;
Fig. 4 is a conceptual diagram showing an example of data stored in a memory circuit shown in Fig. 1; and
Fig. 5 is a flowchart of a state transition during system startup shown in Fig. 1.

BEST MODE FOR EMBODYING THE INVENTION

[0011] Fig. 1 shows an exemplary configuration of a system using a PLD according to the present invention. The system in Fig. 1 includes a PLD 10, a memory circuit 11, and a logic circuit 12, each of which receives power supply voltages Vdd and Vss and a reset (RST) signal. The RST signal stays active (high) for a predetermined period of time during the power-up of the system. The memory circuit 11 contains (for example 1 megabit of) rewritable, nonvolatile memory for storing program data to be programmed in the PLD 10, a clock generator, and a unit for state control and provides a clock (CLK) signal, a control (CTL) signal, and a data (DT) signal to the PLD 10. The PLD 10 receives the DT signal representing th program data in synchronization with the CLK signal while the CTL signal remains active (low). The logic circuit 12, which includes a microprocessor for example, accomplishes a predetermined system function in cooperation with the programmed PLD 10.

[0012] Fig. 2 shows an exemplary internal configuration of the PLD 10 shown in Fig. 1. While the PLD 10 in practice contains a large number of logic arrays (programmable internal logic circuit units), only first and second logic arrays 20, 30 are shown in Fig. 2 for simplicity.

While the PLD 10 has a large number of xt mal pins (for example 240 pins) for connecting the PLD 10 with the logic circuit 12, only two external pins 24, 34 are shown in Fig. 2 for simplicity. Th first logic array 20 is connected to th xternal pin 24 through an xternal pin control circuit 21 containing a selector 22 and through an I/O pad 23. The second logic array 30 is connected to the external pin 34 through an external pin control circuit 31 containing a selector 32 and through an I/O pad 33. The selector 22 selectively communicates a fixed high or low level during system startup and eventually communicates an output from the first logic array 20 to the I/O pad 23 if the external pin 24 is used as an output pin. The selector 32 selectively communicates a fixed high or low level during system startup and eventually communicates an output from the second logic array 30 to the I/O pad 33 if the external pin 34 is used as an output pin. The logic arrays 20, 30 exchange data with each other over a main bus 40. The PLD 10 shown in Fig. 2 further includes a PLD control circuit 41 receiving the CLK signal, CTL signal, and DT signal provided from the memory circuit 11. The PLD control circuit 41 receives the DT signal in synchronization with the CLK signal while the CTL signal stays active (low), and provides program data to the first and second logic arrays 20, 30 and the external pin control circuits 21, 31. Internal circuits in the PLD 10 are initialized by a high RST signal.

[0013] Fig. 3 shows an exemplary internal configuration of the first logic array 20 shown in Fig. 2. The logic array 20 includes a large number of logic units 50. Each logic unit 50 comprises a programmable logic element 51 and a selector 52. A first input of the selector 52 communicates an output from the logic element 51 in the logic unit 50 to the main bus 40 and a second input of the selector 52 is connected to a bypass line 53 for communicating an output from the adjacent logic unit directly to the main bus 40. The logic array 20 also has a selector (not shown) for providing a bypass route for transmitting information received from the main bus 40. The second logic array 30 in Fig. 20 also has a similar bypass route.

[0014] Fig. 4 shows an example of data stored in the memory circuit 11 shown in Fig. 1. As shown in Fig. 4, the program data is divided into a pin setting data block 60 for defining the initial state of the external pins 24, 34, a minimum logic setting data block 61 for defining functions of one or more of the internal logic circuits (the first logic array 20) required during system startup, and a full logic setting data block 62 for defining functions of all the internal logic circuits (the first and second logic arrays 20, 30), in ascending order of address. The program data stored in the minimum logic setting data block 61 is prepared in such a way that the functions of PLD 10 that are required during system startup can be provided through the use of the first logic array 20 alone without the us of the second logic array 30.

[0015] Fig. 5 shows a state transition during startup of the system shown in Fig. 1. The first state S1 is the initial state, the second state S2 is a state in which the pin s tting data block 60 is transferr d, the third sat S3 is a sate in which th minimum logic setting data block 61 is transferred, the fourth state S4 is a first steady state after the functions required for system startup is programmed in the PLD 10, the fifth state S5 is a state in which the full logic setting data block 62 is transferred, and the sixth state S6 is a second steady state after all the functions of the PLD 10 are programmed in the PLD 10. Each of the states will be described below in th order of occurrence.

[0016] During the system in Fig. 1 is powered up, that is, the system is started up, the RST signal remains active (high) for a predetermined period of time. The memory circuit 11 starts to provide the CLK signal in respons to the power-up, and hold the CTL signal inactive (high) in response to the high RST signal. This state is th first state S1, that is, the initial state. In the PLD 10, all selectors 52 of each of the first and second logic arrays 20 and 30 select the bypass line 53 in response to the high RST signal. Therefore, all the logic elements 51 are disconnected from the main bus 40. The external pin control circuits 21, 31 set the attribute of all the external pins 24, 34 as an "Input" pin and cause all the selectors 22, 32 to select the fixed low input. Alternatively, they may cause all the selectors 22, 32 to select the fixed high input.

[0017] When the RST signal becomes inactive (low), the memory circuit 11 changes the CTL signal to active (low) and continues providing the CLK signal whil sequentially providing a DT signal concerning the pin setting data block 60 to the PLD 10 in synchronization with the CLK signal. This is the second state S2. In th PLD 10, the PLD control circuit 41 receives the DT signal in synchronization with the CLK signal while monitoring the low CTL signal and provides pin setting data to the external pin control circuits 21, 31. The pin setting data is a set of pin attribute and pin value of each pin. This decides the state of all the external pins 24, 34. In particular, the logical level of an external pin of which th attribute is set as an "output" pin is settled at a predetermined pin value (high or low selected by the sel ctor 22 or 32). Therefore, even if both of the first and second logic arrays 20, 30 are in an unstable (undefined) state, the unstable state does not propagate to the logic circuit 12.

[0018] After the states of all the external pins 24, 34 are set, the third state S3 is entered. In the third state S3, the memory circuit 11 sequentially provides a DT signal concerning the minimum logic setting data block 61 to the PLD 10 in synchronization with the CLK signal while holding the CTL signal active (low). In the PLD 10, the PLD control circuit 41 receives the DT signal in synchronization with the CLK signal while monitoring the low CTL signal, and provides the minimum logic setting data to th first logic array 20. This decid s th circuit configuration of the first logic array 20 for providing functions required for system startup (functions required for

a stable operation of the system). However, the state of the second logic array 30 is still unstabl .

[0019] After the transfer of th minimum logic setting data block 61 is completed, the memory circuit 11 first forces the CTL signal back to inactive (high). This state is the fourth state S4, that is, the first steady stat . The first logic array 20, of which the functions have been already defined, can access the external pin 34 over a bypass route in the second logic array 30. The logic circuit 12 shown in Fig. 1 can receive information from the PLD 10 in the first steady state through the external pins 24, 34. Therefore, the logic circuit 12 can be initialized according to the state of the PLD 10.

[0020] When a stage in which the system uses all the functions of the PLD 10 is reached, the memory circuit 11 forces the CTL signal back to active (low), then sequentially provides to the PLD 10 a DT signal concerning the full logic setting data block 62 in synchronization with the CLK signal. This state is the fifth state S5. In the PLD 10, the PLD control circuit 41 receives the DT signal in synchronization with the CLK signal while monitoring the low CTL signal, and provides the full logical setting data to the first and second logic arrays 20, 30. This decides the final circuit configuration of the first and second logic arrays 20, 30.

[0021] After the completion of the transfer of the full logic setting data block 62, the memory circuit 11 forces the CTL signal back to inactive (high). This is the sixth state S6, that is, the second steady state. Then, the logic circuit 12 and the programmed PLD 10 cooperate to accomplish predetermined system functions.

[0022] As described above, the transfer of the pin setting data block 60 is completed in the earlier, second state S2 in the system including the PLD 10 of the present invention, therefore a time period in which the PLD 10 is unstable during system startup is reduced. In addition, the transfer of the minimum logic setting data block 61 preceding the transfer of the full logic setting data block 62 is completed in the third state S3, therefore the logic circuit 12 can reference the state of the PLD 10 in an early stage during system startup. The amount of data in the pin setting data block 60 may vary depending on the number of external pins of the PLD 10 and the amount of data in the minimum logic setting data block 61 may vary depending on the size of the internal logic circuit and system specifications of the PLD 10.

INDUSTRIAL APPLICABILITY

[0023] According to the present invention, the PLD receives the pin setting data block before receiving the logic setting data block, thereby r ducing a period in which the state of the PLD is unstable during system startup.

[0024] According to the present invention, the PLD r - ceives the minimum logic setting data block before receiving the full logic setting data block, therefore logic circuits adjacent to the PLD can referenc the state of the PLD in an early stage during system startup. In particular, a device recognition system can ref rences the state of the PLD in an early stag in a configuration in which the PLD is connect d onto a bus within an electronic circuit system such as a personal computer.

Claims

1. A method for programming a programmable logic device (PLD), comprising the steps of :

   transferring a pin setting data block for defining an initial state of each of a plurality of external pins of said PLD to said PLD; and
   transferring a logic setting data block for defining functions of an internal logic circuit of said PLD to said PLD after the completion of th transfer of said pin setting data block.

2. A method for programming a programmable logic device (PLD), comprising the steps of:

   transferring to said PLD a minimum logic setting data block for defining functions of on or more of internal logic circuits of said PLD, said one or more of internal logic circuits being required in starting up a system containing said PLD; and
   transferring to said PLD a full logic setting data block for defining functions of all the internal logic circuits of said PLD after the compl tion of the transfer of said minimum logic setting data block.

3. A method for programming a programmabl logic device (PLD), comprising the steps of:

   transferring a pin setting data block for defining an initial state of each of a plurality of ext rnal pins of said PLD to said PLD;
   transferring to said PLD a minimum logic setting data block for defining functions of ne or more of internal logic circuits of said PLD after the completion of the transfer of said pin setting data block, said one or more of internal logic circuits being required in starting up a system containing said PLD; and
   transferring a full logic setting data block for defining functions of all the internal logic circuits of said PLD to said PLD after the completion of the transfer of said minimum logic setting data block.

4. A programmable logic device, **charact riz d in that** the programmable logic device receives a pin setting data block for defining an initial state of each

of a plurality of external pins before receiving a logic setting data block for defining functions of an int r-nal logic circuit.

5. A Programmable logic device, **characterized in that** the programmable logic device receiv s a minimum logic setting data block for defining functions of one or more of internal logic circuits before receiving a full logic setting data block for defining functions of all the internal logic circuits, said one or more of internal logic circuits being required in system startup.

6. A programmable logic device, **characterized in that** the programmable logic device, after receiving a pin setting data block for defining an initial state of each of a plurality of external pins, receives a minimum logic setting data block for defining functions of one or more of internal logic circuits before receiving a full logic setting data block for defining functions of all the internal logic circuits, said one or more of internal logic circuits being required in system startup.

Fig. 1

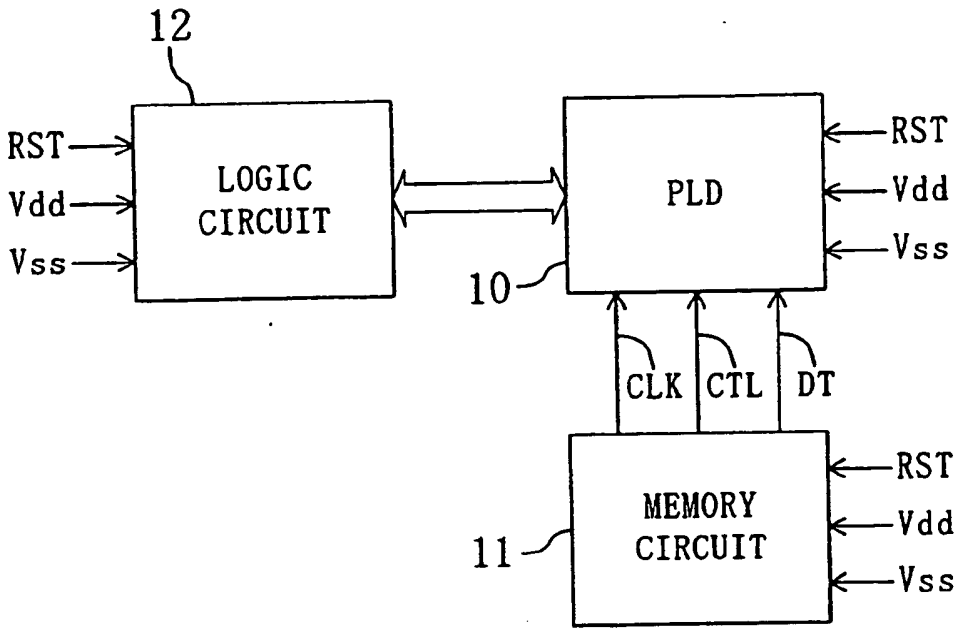

12
RST
Vdd
Vss
LOGIC CIRCUIT
PLD
RST
Vdd
Vss
10
CLK
CTL
DT
MEMORY CIRCUIT
11
RST
Vdd
Vss

Fig. 4

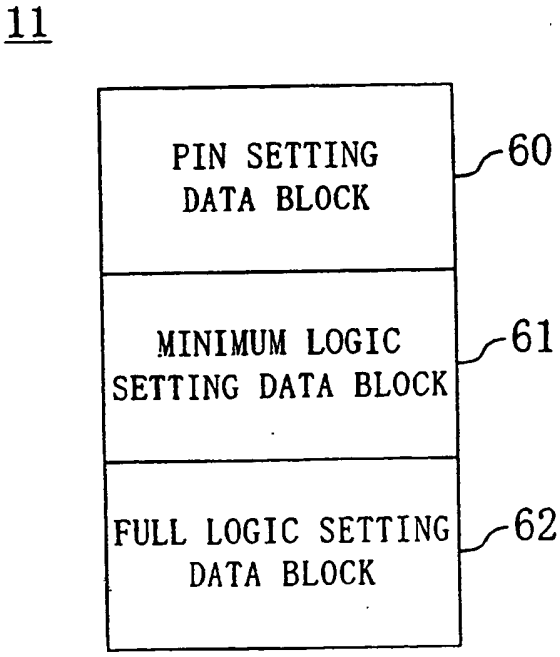

11
PIN SETTING DATA BLOCK
60
MINIMUM LOGIC SETTING DATA BLOCK
61
FULL LOGIC SETTING DATA BLOCK
62

Fig. 2

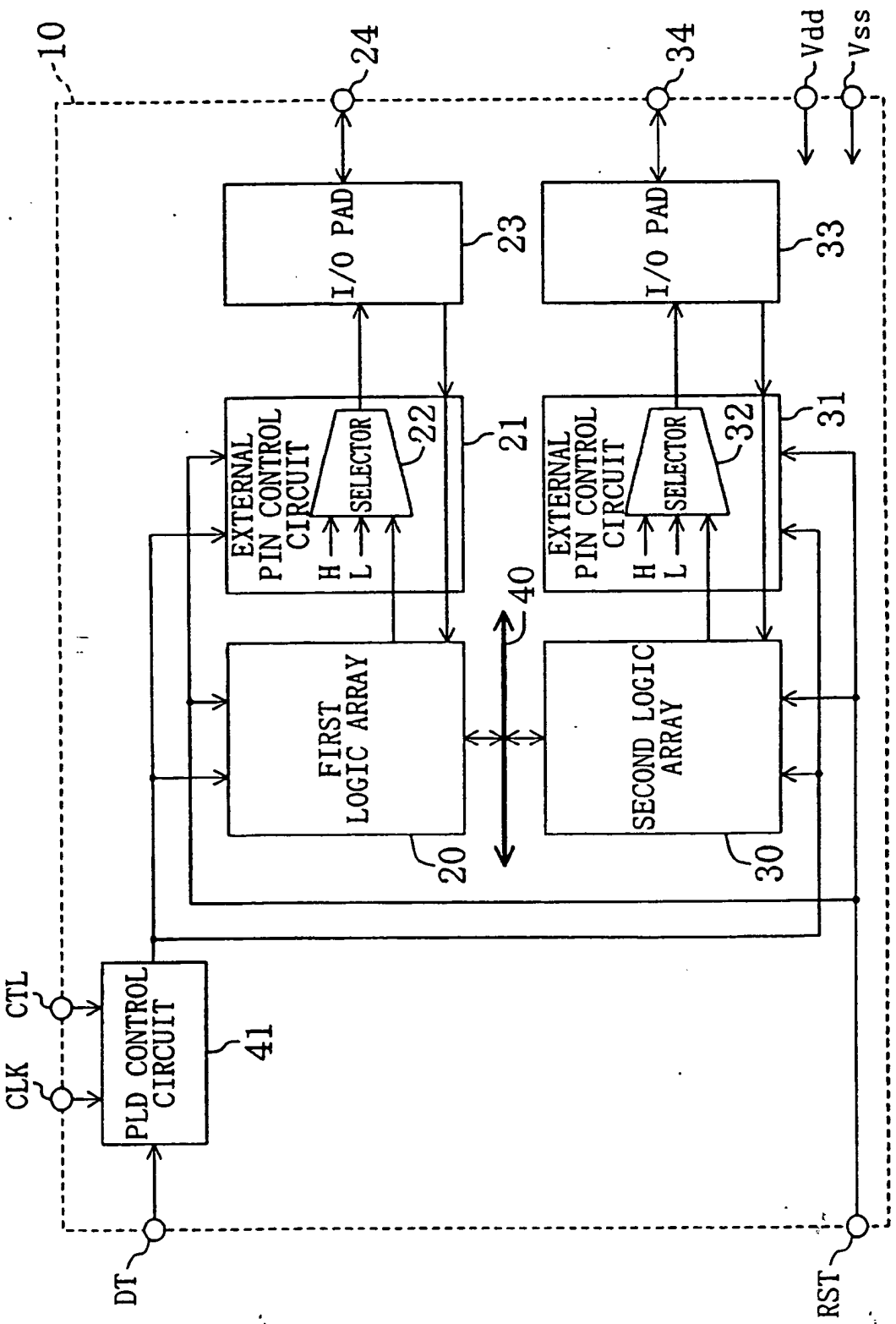

10
24
34
Vdd
Vss
I/O PAD
23
I/O PAD
33
EXTERNAL PIN CONTROL CIRCUIT
SELECTOR
22
21
EXTERNAL PIN CONTROL CIRCUIT
SELECTOR
32
31
H
L
H
L
40
FIRST LOGIC ARRAY
SECOND LOGIC ARRAY
20
30
CLK
CTL
PLD CONTROL CIRCUIT
41
DT
RST

Fig. 3

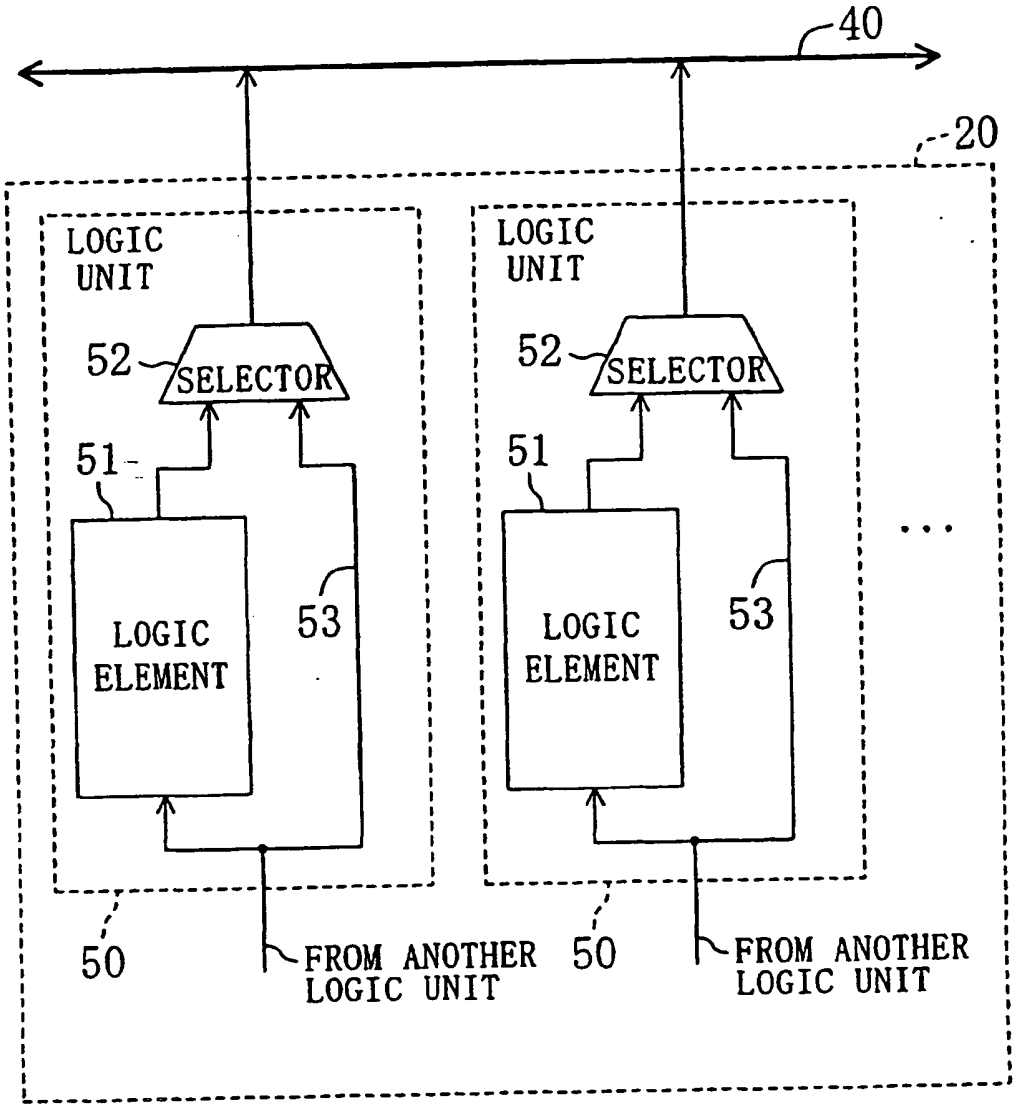
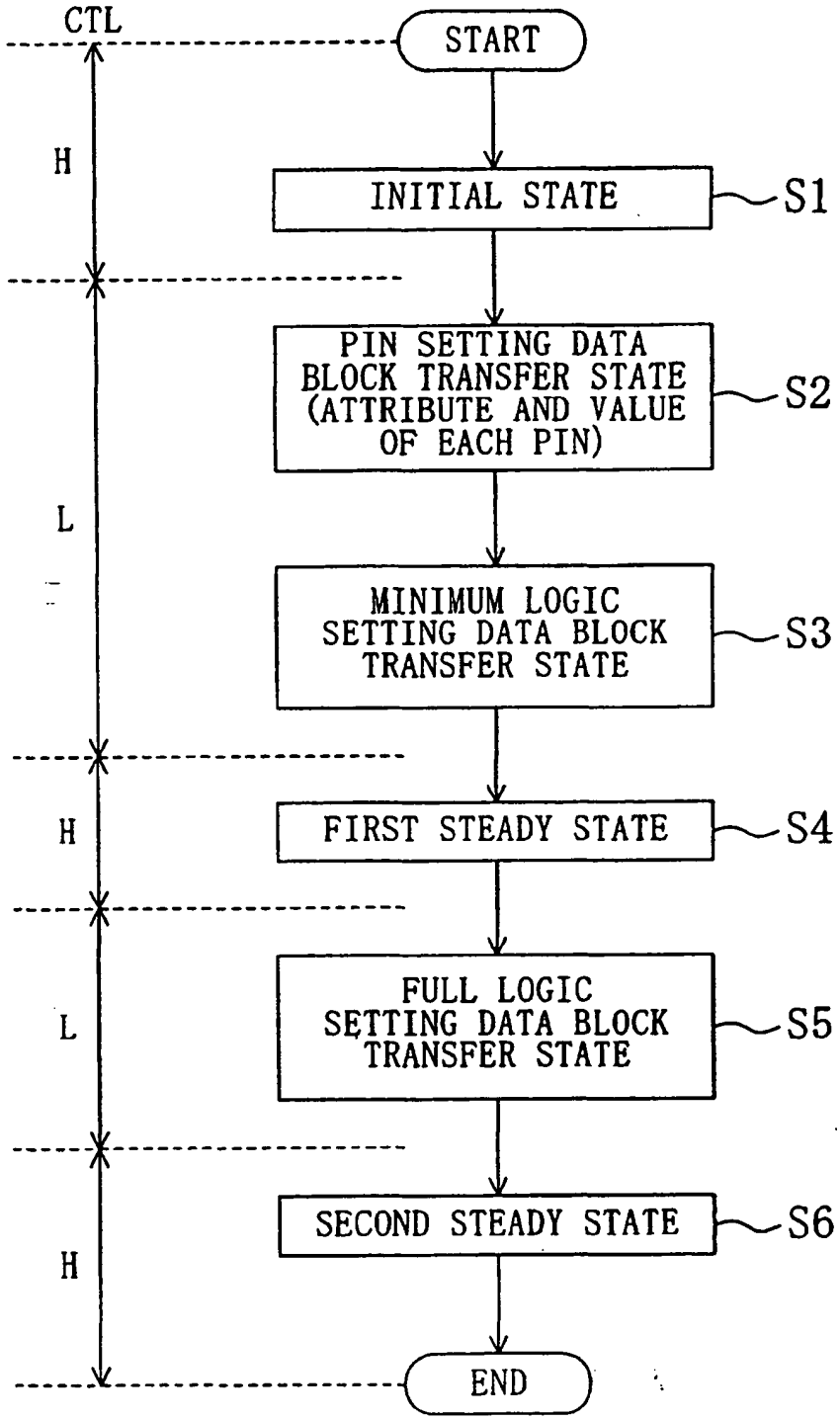

40
20
LOGIC UNIT
52
SELECTOR
51
LOGIC ELEMENT
53
50
FROM ANOTHER LOGIC UNIT
LOGIC UNIT
52
SELECTOR
51
LOGIC ELEMENT
53
50
FROM ANOTHER LOGIC UNIT

Fig. 5


CTL
START
H
INITIAL STATE
S1
PIN SETTING DATA BLOCK TRANSFER STATE (ATTRIBUTE AND VALUE OF EACH PIN)
S2
L
MINIMUM LOGIC SETTING DATA BLOCK TRANSFER STATE
S3
H
FIRST STEADY STATE
S4
L
FULL LOGIC SETTING DATA BLOCK TRANSFER STATE
S5
H
SECOND STEADY STATE
S6
END

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/08032

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl^{7} H03K19/173

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl^{7} H03K19/173

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho(Y1,Y2) 1926-2000 Toroku Jitsuyo Shinan Koho(U) 1994-2000
Kokai Jitsuyo Shinan Koho(U) 1971-2000 Jitsuyo Shinan Toroku Koho(Y2) 1996-2000

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP, 11-74360, A (NEC Kansai, Ltd.), 16 March, 1999 (16.03.99), Full text, & US, 6147509	1,4 1-6
X Y	JP, 8-307246, A (NEC Eng. Ltd.), 22 November, 1996 (22.11.96), Par. Nos. [0009] to [0016] (Family: none)	2,5 1-6
A	JP, 11-225063, A (NEC IC Microcomput. System Ltd.), 17 August, 1999 (17.08.99), Full text (Family: none)	1-6
A	JP, 11-274915, A (Victor Company of Japan, Limited), 08 October, 1999 (08.10.99), Full text (Family: none)	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 January, 2001 (28.01.01)	30 January, 2001 (30.01.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/08032

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. The inventions of claims 1, 4 relate to a PLD and PLD setting method for transferring a pin setting data block before setting a function of an internal logic circuit of the PLD.

2. The inventions of claims 2, 5 relate to a PLD and PLD setting method for first transferring a minimum logic setting data block for defining the functions of part of the internal logic circuits necessary at the start up of the system including the PLD out of all the internal logic circuits of the PLD.

3. The inventions of claims 3, 6 relate to a combination of the inventions of claims 1, 2.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest
☐ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet (1)) (July 1992)